IN THE DRAWINGS:

Attached are three (3) Annotated Sheets and three (3) Replacement Sheets. Please substitute original Formal Drawing sheets 2, 3 and 4 with the Replacement Sheets 2, 3 and 4 attached hereto.

REMARKS

In the Office Action, the Examiner rejected Claims 1-16, which were all of the then pending claims, under 35 U.S.C. §102 as being fully anticipated by U.S. Patent 5,666,078 (Lamphier, et al.). The Examiner also raised objections to the drawings and to the specification.

Applicants are herewith filing a Request for Continued Examination to continue the prosecution of this application.

With respect to the drawings, the Examiner, in the Office Action, objected to Applicants' earlier corrections to Figure 2 on the grounds that the changes did not satisfy the requirements for formal drawings. The Examiner suggested making these changes to the formal drawings filed on February 7, 2002. The Examiner also noted that in Figure 3, "16" should be "12" and that in Figure 2B, "PVDRIVE" should be "PNDRIVE".

Replacement sheets showing these corrections to Figures 2A, 2B and 3 are being submitted herewith. Accordingly, the Examiner is asked to reconsider and to withdraw the objections to the drawings.

With regard to the specification, the Examiner observed that on page 3, line 8, "Figure 2 is" should be changed to "Figures 2, 2A and 2B are", and that on page 4, line 1, "controller I/O cell 16" should be changed to "controlled I/O cell 12". This opportunity is being taken to make these changes to pages 3 and 4, and the Examiner is thus requested to reconsider and to withdraw the objections to the specification.

Also, in order to better define the subject matters of the claims, new independent Claims 17 and 18 are being added as substitutes for Claims 1 and 9 respectively, which are being cancelled. Claims 2, 4, 5 and 7 are being amended to be dependent from Claim 17 instead of Claim 1; and Claims 10, 12, 13, 15 and 16 are being amended to be dependent from Claim 18 instead of Claim 9. Thus, as presented herein, Claims 2-8 are dependent from Claim 17 and Claims 10-16 are dependent from Claim 18.

In addition, Claims 2-4, 7 and 8 are being amended to keep the language of these claims consistent with the language of Claim 17. Similarly, Claims 10-12 and 14-16 are being amended to keep the language of these claims consistent with the language of Claim 18. New independent Claims 19 and 20 are being added to describe the invention in an alternative way.

For the reasons set forth below, Claims 2-8 and 10-20 patentably distinguish over the prior art and are allowable. The Examiner is, thus, respectfully requested to reconsider and to withdraw the rejection of Claims 2-8 and 10-16 under 35 U.S.C. §102, and to allow these claims and new Claims 17-20.

As discussed in detail in the present application, this invention generally relates to an I/O cell having a programmable active input bias. In accordance with this invention, a digital controller and a reference cell are used to determine the extent to which a driver impedance on the I/O cell should be adjusted, and then the controller sends a signal to the I/O cell to so adjust that driver impedance.

More specifically, the reference cell includes a node having a variable voltage, and the digital controller generates a first signal and applies that signal to the reference cell to change the voltage of that node. The voltage of the node is compared to a reference voltage, and the digital controller then generates a second signal based on that comparison. This second signal has an adjustable value, and the controller adjusts that value until it reaches a stable value.

This second signal is applied to the I/O cell to adjust the impedance of the driver of the I/O cell. A third signal may be applied, preferably by the digital controller, to the I/O cell, during a defined period of time, to prevent the I/O cell from receiving the second signal until the value of that second signal becomes stable.

In the preferred embodiment of this invention, described in the present application, this third signal is referred to as the "NOUPDT" signal. In its preferred implementation, the input "NOUPDT" is a strobe input from the digital controller. When NOUPDT (no-update) is asserted, the I/O will not accept the control bits PVTN[5:0] and PVTP[5:0]. The signal NOUPDT is asserted before the controller sends out new values of control bits and stays asserted until all bits are stable. This prevents glitching of the I/O impedance when the control bit values are changing.

The prior art of record fails to disclose or suggest the use of this third signal.

In particular, Lamphier, et al. discloses an output driver circuit having a programmable impedance. Voltage from an external resistance device is compared with a voltage developed by an evaluate circuit. A control logic adjusts the evaluate circuit with a count until the two voltages are basically equal. At this time, the control logic, using this count, operates an off chip driver circuit to produce a desired driving input. There is no disclosure or suggestion in

Lamphier, et al, though, of applying this count value to the driver and also applying another signal to the driver to prevent the driver from accepting that count signal until that count signal become stable.

New independent Claims 17 and 18 clearly describe this difference between the present invention and the Lamphier, et al. Specifically, new Claim 17, which is directed to a method of controlling the impedance of a driver of an input/output cell, describes the feature of applying a third signal to the input/output cell, during a defined period of time, to prevent the input/output cell from receiving the second signal until the value of that second signal becomes stable. New Claim 18, which is directed to an application specific integrated circuit comprising an I/O cell including a driver with an adjustable impedance, describes an analogous apparatus feature.

The other references of record have been reviewed, and these other references, whether they are considered individually or in combination also fail to disclose or suggest this feature of the present invention.

For example, Otsuka, et al. describes a semiconductor device having an output impedance controller for controlling the impedance of an output buffer. The impedance controller has an external resistor and two dummy buffers. The impedance of the dummy buffers is adjusted to determine an appropriate impedance value for the output buffer. Plainly, however, Otsuka, et al does not teach or suggest using any signal similar or analogous to the above-described third signal of this invention.

In light of the above-discussed differences between Claims 17 and 18 and the prior art, and because of the advantages associated with those differences, Claims 17 and 18 patentably distinguish over the prior art and are allowable. Claims 2-8, 19 and 20 are dependent from, and are allowable with, Claim 17; and Claims 10-16 are dependent from Claim 18 and are allowable therewith. Consequently, the Examiner is respectfully requested to reconsider and to withdraw the rejection of Claims 2-8 and 10-16 under 35 U.S.C. §102, and to allow these claims and new Claims 17 and 18.

In addition, with another feature of the preferred embodiment of the invention, the above-mentioned second signal may be held by the I/O cell until a predetermined condition occurs, at which time the second signal may be applied to the driver of the I/O cell to adjust the impedance of that driver. New Claims 19 and 20 describe this feature. Holding this second signal in this way also is not disclosed or suggested by the prior art. This feature also helps to prevent glitching of the I/O impedance control circuit when the control bit values are changing. Accordingly, independent Claims 19 and 20 also patentably distinguish over the prior art and are allowable.

For the reasons set forth above, the Examiner is asked to reconsider and to withdraw the objections to the drawings and to the specification. The Examiner is also asked to reconsider and to withdraw the rejection of Claims 2-8 and 10-16 under 35 U.S.C. §102, and to allow Claims 2-8 and 10-20.

If the Examiner believes that a telephone conference with Applicants' Attorneys would be advantageous to the disposition of this case, the Examiner is requested to telephone the undersigned.

Respectfully submitted,

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JSS:jy
Enclosures: Three (3) Annotated Sheets 2, 3 and 4 of the Formal Drawings; and
Three (3) Replacement Sheets 2, 3 and 4 of the Formal Drawings.

ANNOTATED SHEET

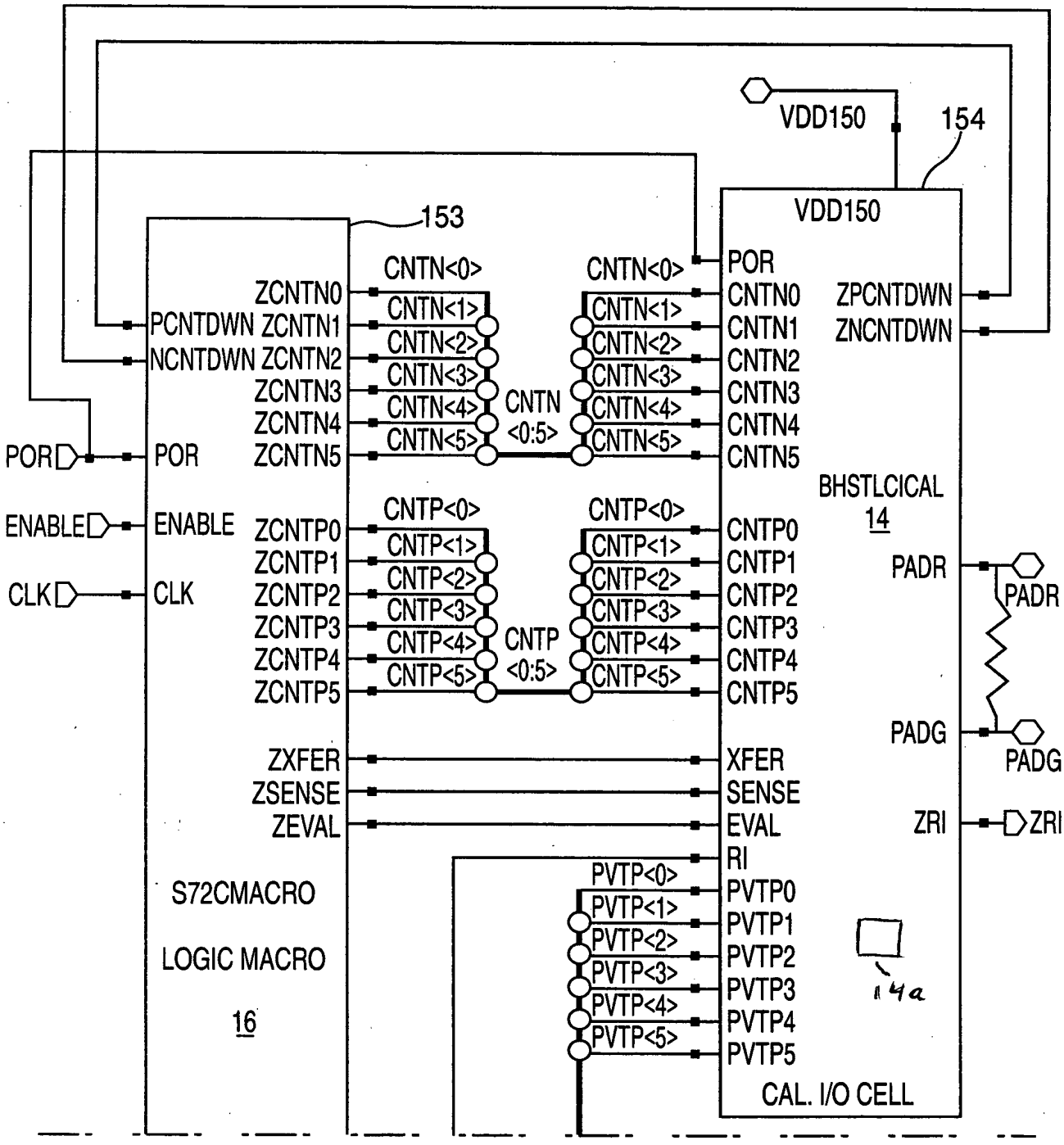


FIG. 2A

2-A
2-B

FIG. 2

ANNOTATED SHEET

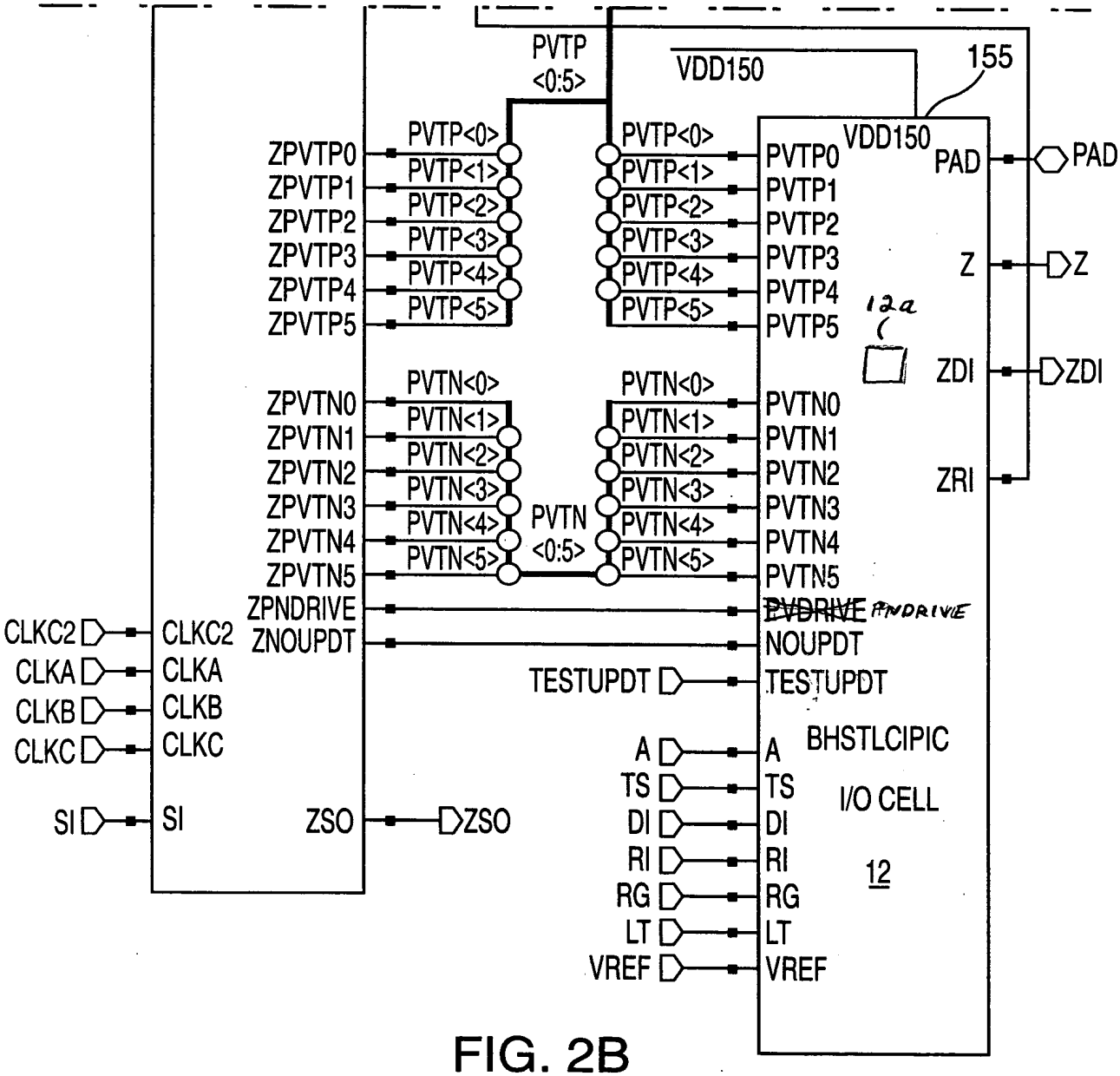
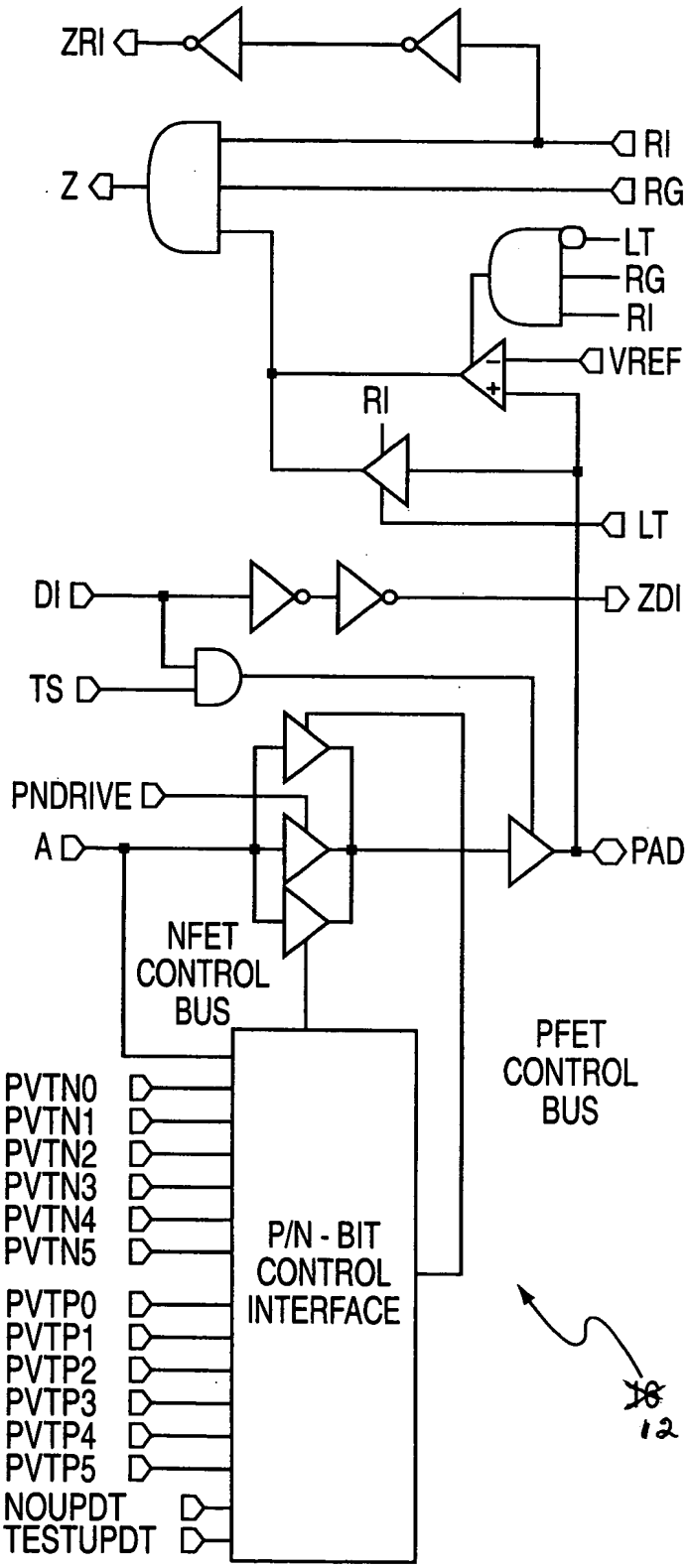


FIG. 2B

ANNOTATED SHEET

A	DRIVER DATA INPUT
TS	DRIVER TRI-STATE CONTROL
DI	DRIVER INHIBIT INPUT (DI IN)
LT	DC CURRENT GATE (I_{dd} TEST) INPUT
RI	RECEIVER INHIBIT INPUT (RI IN)
RG	RECEIVER GATE CONTROL
VREF	VOLTAGE REFERENCE INPUT
PAD	DRIVER OUTPUT/RECEIVER INPUT
ZDI	DRIVER INHIBIT OUTPUT (DI OUT)
ZRI	RECEIVER INHIBIT OUTPUT (RI OUT)
Z	RECEIVER OUTPUT
PVTN0	NFET PVT CONTROL BIT (LSB)
PVTN1	NFET PVT CONTROL BIT
PVTN2	NFET PVT CONTROL BIT
PVTN3	NFET PVT CONTROL BIT
PVTN4	NFET PVT CONTROL BIT
PVTN5	NFET PVT CONTROL BIT (MSB)
PVTP0	PFET PVT CONTROL BIT (LSB)
PVTP1	PFET PVT CONTROL BIT
PVTP2	PFET PVT CONTROL BIT
PVTP3	PFET PVT CONTROL BIT
PVTP4	PFET PVT CONTROL BIT
PVTP5	PFET PVT CONTROL BIT (MSB)
PNDRIVE	DEFAULT CONTROL BIT
NOUPDT	PREVENTS BIT UPDATE
TESTUPDT	UPDATES BITS



CONTROLLED I/O CELL

FIG. 3